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CAT # LCD-58

MODEL	HG25504NG-01	2/28	PRODUCT SPECIFICATIONS
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1. FEATURES

- * The features of HG25504NG-01 are as follows :
- * Display mode : STN gray positive type display
- * Display format : 256 × 128 Dots
- * Driving method : 1/128 Duty
- * Viewing direction : 6 O'clock
- * 80 Serise available

2. MECHANICAL SPECIFICATIONS

Item	Specification	Unit
Module Size (W × H × T)	147.0 × 116.0 × 12.0 Max	mm
Viewing Area (W × H)	127.0 × 70.0	mm
Dot Size (W × H)	0.43 × 0.43	mm
Dot Pitch (W × H)	0.47 × 0.47	mm
Weight	About 155	g

3. ABSOLUTE MAXIMUM RATINGS

3-1. Electrical Absolute Maximum Ratings

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.-		
Supply voltage	Logic	$V_{DD} - V_{SS}$	0	-	7.0	$T_a=25^\circ\text{C}$ $V_{DD}=5V \pm 10\%$ $V_{SS}=0V$
	LCD	$V_{DD} - V_0$	0	-	30	
Input voltage	V_i	-0.3	-	$V_{DD}+0.3$	V	

3.2 Environmental conditions

Item	Symbol	Min.	Max.	Unit
Operating temperature	Topr	0	50	°C
Storage temperature	Tstg	-20	70	°C
Humidity (Ambient temperature=Ta)	Ta ≤ 40°C		95% RH max.	
	Ta > 40°C (Below maximum temp.)		Absolute humidity shall be less than Ta=40°C, 95% RH	

4. ELECTRICAL CHARACTERISTICS

Item	Symbol	Spec. Value			Unit	Condition	
		Min.	Typ.	Max.			
Supply voltage	Logic	VDD - VSS	4.5	5.0	5.5	V	-
	LCD	VDD - VO	-	16.5	-	V	Ta = 0 °C
			14.3	15.1	15.9	V	Ta = 25 °C
			-	13.7	-	V	Ta = 50 °C
Supply Current	Logic	IDD	-	10.0	15.0	mA	Note 1)
	LCD	IO	-	5.0	7.5	mA	
Input voltage	High level	VIH	0.8 VDD	-	VDD	V	-
	Low level	VIL	0	-	0.2 VDD	V	-

Note 1) Condition : VDD = 5 V

VDD - VO = 15.1V

Display pattern : Full dot ON

5. OPTICAL CHARACTERISTICS

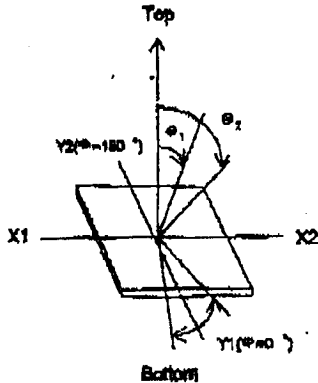
Ta = 25°C, VDD = 5V ± 10%

Item	Symbol	Min.	Typ.	Max.	Unit	Condition	Note	
Viewing angle	$\theta_2 - \theta_1$	$\theta = 0^\circ$ (Y1-Y2)	50	60	-	deg.	Cr = 1.4	1,2
		$\theta = 90^\circ$ (X1-X2)	50	60	-			
Contrast ratio	Cr	2	4	-	-	$\theta = 0^\circ$ $\phi = 0^\circ$	3	
Response time(rise)	Tr	-	130	230	ms	$\theta = 0^\circ$ $\phi = 0^\circ$	4	
Response time(fall)	Tf	-	150	250	ms	$\theta = 0^\circ$ $\phi = 0^\circ$	4	

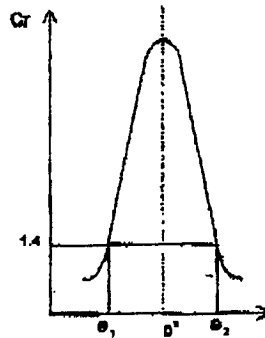
* Above datas are measured under 1/128 duty STN gray positive mode.

* $\theta = 0^\circ$, $\phi = 90^\circ$ means viewing direction.

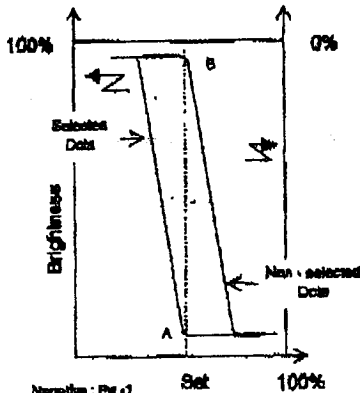
Note 1. Definition of angle θ and ϕ



Note 2. Definition of viewing angle θ_1 and θ_2

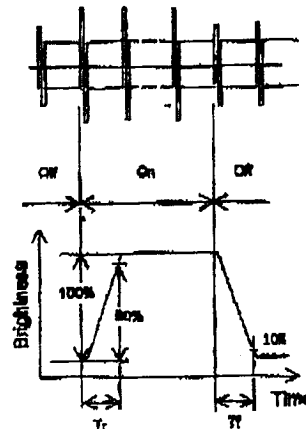


Note 3. Definition of contrast Cr



$C = (A/B)^*$ { Negative : $\theta = 0^\circ$
Positive : $\theta = 90^\circ$

Note 4. Definition of Optical response



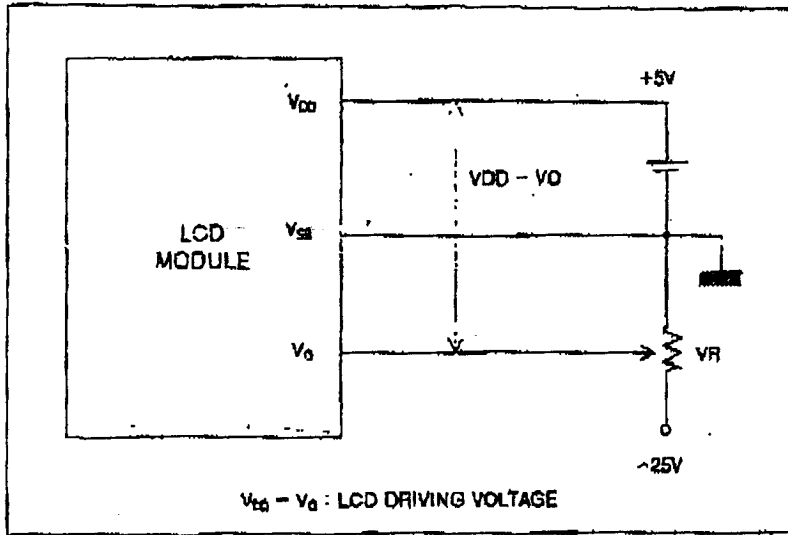
6. INTERFACE PIN ASSIGNMENT

Pin No.	Symbol	Level	Function
1	FG	0V	Frame ground
2	V _{SS} (GND)	0V	Ground
3	V _{DD} (V _{CC})	+5V	Power supply voltage for logic and LCD
4	V ₀	-	Operating voltage for LCD (variable)
B4	/RES	H/L	Reset signal
B5	/RD	H/L	Read signal
B6	/WR	H/L	Write signal
B5	/CS	H/L	Chip select signal
D0	A0	H/L	Data type select signal
D0	DB0	H/L	Display data bit 0
D1	DB1	H/L	Display data bit 1
D2	DB2	H/L	Display data bit 2
D3	DB3	H/L	Display data bit 3
D4	DB4	H/L	Display data bit 4
D5	DB5	H/L	Display data bit 5
D6	DB6	H/L	Display data bit 6
D7	DB7	H/L	Display data bit 7

*Sel 1
 and
 Sel2 are already tied to GND*

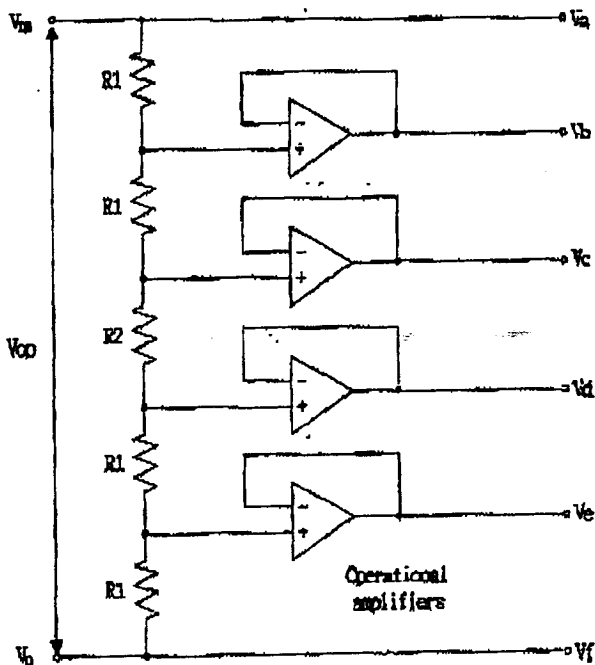
*Separate Function
 /RD
 /WR*

7. POWER SUPPLY BLOCK DIAGRAM



8. BIAS VOLTAGE GENERATION CIRCUIT

Six levels of voltage, V_a to V_f are applied to the common and segment drivers. The voltage is generated through operational amplifier by resistance-division from liquid crystal operating voltage (V_{op}). Here, an operation amplifier is used as a voltage follower.



V_a	Common and segment selection high level
V_b	Common non-selection high level
V_c	Segment non-selection high level
V_d	Segment non-selection low level
V_e	Common non-selection low level
V_f	Common and segment selection low level

9. TIMING CHARACTERISTICS

9-1. Interface timing chart (8080 family interface)

$V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$

Signal	Symbol	Parameter	Rating		Unit
			Min.	Max.	
AO, /CS	tAH	Address hold time	10	-	.CL = 100pF+1 TTL load
	tAW	Address setup time	30	-	
/WR, /RD	tCYC	System cycle time	Note1)	-	
	tCC	Strobe pulse width	220	-	
D0 - D7	tDS	Data setup time	120	-	
	tDH	Data hold time	10	-	
	tACC	/RD access time	-	120	
	tOH	Output disable time	10	50	

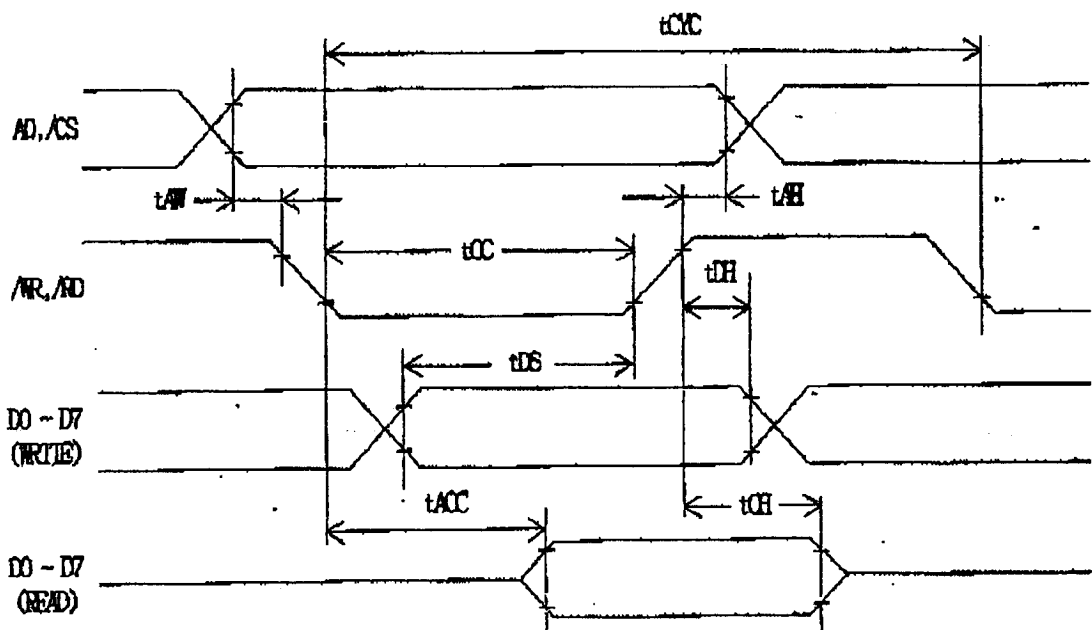
Note1)

For memory control and system control commands:

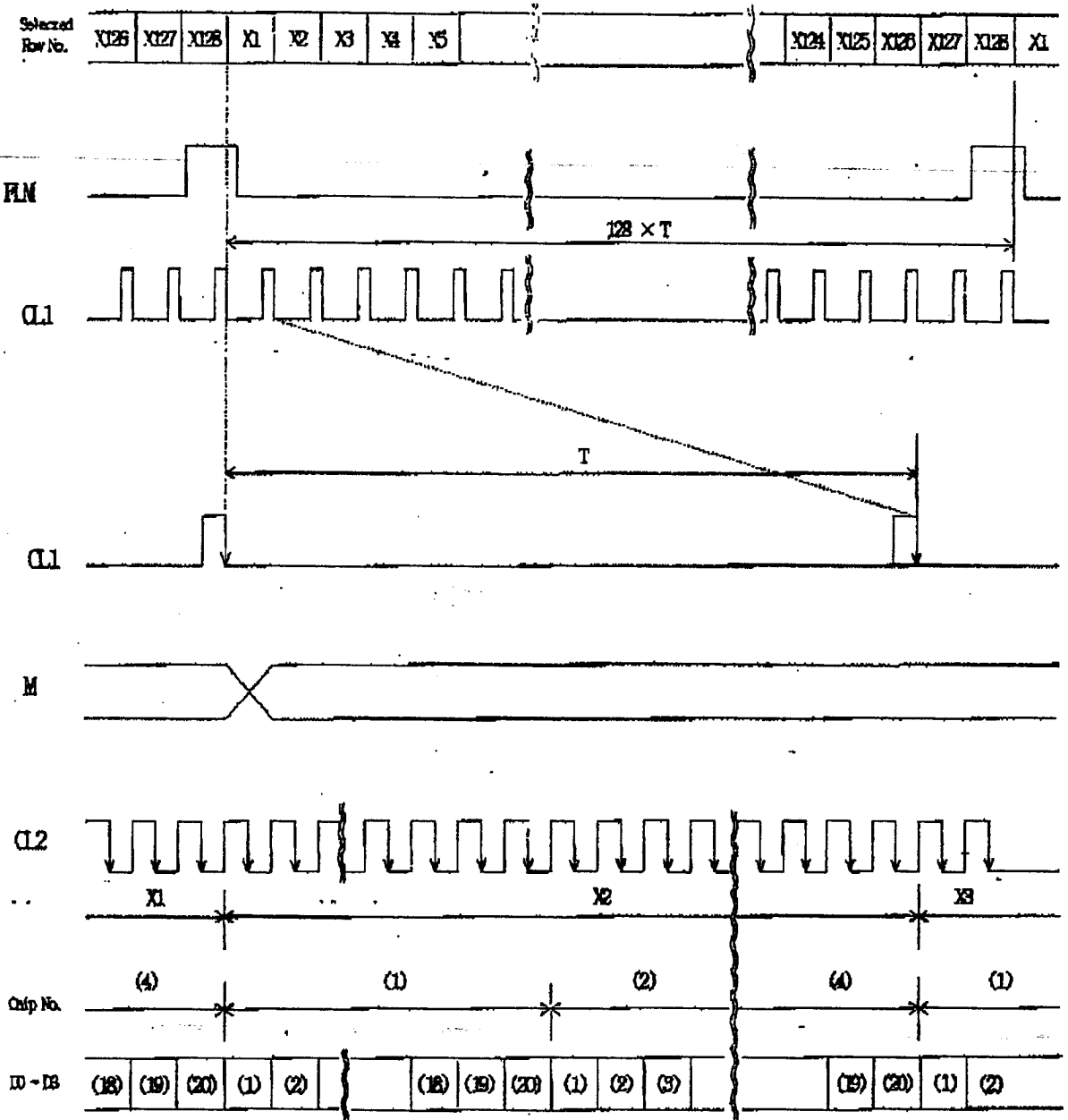
$$t_{CYC} = 4t_C + t_{CC} - 45 > 3t_C + 125$$

For all other commands:

$$t_{CYC} = 4t_C + t_{CC} + 30$$



9-2. AC electrical characteristics



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10. INSTRUCTION SETS

Class	Command	CODE												Hex	Description
		/RD	/WR	A0	D7	D6	D5	D4	D3	D2	D1	D0			
System Control	SYSTEM SET	1	0	1	0	1	0	0	0	0	0	0	0	40	Initialize device and display.
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Enter standby mode.	
Display Control	DISP ON/OFF	1	0	1	0	1	0	1	1	0	0	D	58 59	Enable and disable display and display flashing.	
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Set display start address and display regions.	
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Set cursor type.	
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Set start address of character generator RAM.	
	CSRDIR	1	0	1	0	1	0	0	1	1	C D 1	C D 0	4C to 4F	Set direction of cursor movement.	
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Set horizontal scroll position.	
	OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Set display overlay format.	
Drawing Control	CSRW	1	0	1	0	1	0	0	0	1	1	0	46	Set cursor address.	
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Read cursor address.	
Memory Control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Write to display memory.	
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Read from display memory.	

10-1. SYSTEM CONTROL COMMANDS

10-1-1. SYSTEM SET

Initializes the device, sets the window sizes and selects the LCD interface format. Since this command sets the basic operating parameters of the LCD module (HG25504NG-01), an incorrect SYSTEM SET command may cause other commands to operate incorrectly.

	MSB				LSB			
	D7	D6	D5	D4	D3	D2	D1	D0
C	0	1	0	0	0	0	0	0
P1	0	1	IV	1	W/S	N2	M1	NO
P2	WF	0	0	0	← FX →			
P3	0	0	0	0	← FY →			
P4	← C/R →							
P5	← TC/R →							
P6	← L/F →							
P7	← APL →							
P8	← APB →							

10-1-1-1. C

This control byte performs the following.

1. Resets the internal timing generator.
2. Disables the display.
3. Cancels sleep mode.

The parameters following P1 are not needed to cancel sleep mode.

10-1-1-2. NO

Selects the internal or external character generator ROM. The internal character generator ROM contains 160, 5×7-pixel characters as shown in character font. These characters are fixed at fabrication by the metalization mask. The external character generator ROM, on the other hand, can contain up to 256 user-defined characters.

NO = 0 : Internal CG ROM
 NO = 1 : External CG ROM

Note that if the CG ROM address space overlaps the display memory address space, that portion of the display memory cannot be written to.

10-1-1-3. M1

Selects the memory configuration for user-definable characters. The CG RAM codes select one of the 64 codes. (M1=0) No D6 correction
 The CG RAM1 and CG RAM2 address spaces are not contiguous.

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The CG RAM1 address space is treated as character generator RAM and the CG RAM2 address space is treated as character generator ROM.

M1 = 1 : D6 correction

The CG RAM1 and CG RAM2 address spaces are contiguous and both treated as character generator RAM.

10-1-1-4. M2

Selects the height of the character bitmaps. Characters more than 16 pixels high can be displayed by creating a bitmap for each portion of each character and using the LCD module's graphics mode to reposition them.

M2 = 0 : 8-pixel character height.

M2 = 1 : 16-pixel character height.

10-1-1-5. W/S

Selects the LCD drive method.

W/S = 0 : Single-panel drive

W/S = 1 : Two-panel drive

10-1-1-6. IV

Screen origin compensation for inverse display. IV is usually set to 1.

The best way of displaying inverted characters is to Exclusive-OR the text layer with the graphics background layer. However, inverted characters at the top or left of the screen are difficult to read as the character origin is at the top-left of its bitmap and there are no background pixels either above or to the left of these character.

The IV flag causes the LCD module to offset the text screen against the graphics back layer by one vertical pixel.

Use the horizontal pixel scroll function (HDOT SCR) to shift the text screen 1 to 7 pixels to the right. All characters will then have the necessary surrounding background pixels that ensure easy reading of the inverted characters.

IV = 0 : Screen top-line correction

IV = 1 : No screen top-line correction

10-1-1-7. FX

Defines the horizontal character size as shown in the following table. The character width in pixels is equal to FX + 1, where FX can range from 00 to 07H inclusive. If data bit 3 is set (FX is in the range 08 to 0FH) and an 8-pixel font is used, a space is inserted between characters.

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HEX	FX				[FX] character width(pixels)
	D3	D2	D1	D0	
00	0	0	0	0	1
01	0	0	0	1	2
	↓	↓	↓	↓	↓
07	0	1	1	1	8

FX

since the LCD module handles display data in 8-bit units, characters larger than 8-pixels wide must be formed from 8-pixel segments.

In graphics mode, the normal character field is also 8-pixels. If a wider character field is used, any remainder in the second 8-bits is not displayed.

10-1-1-8. WF

Selects the AC frame drive waveform period, WF is usually set to 1.

WF = 0 : 16-line AC drive

WF = 1 two-frame AC drive

In two-frame AC drive, the WF period is twice the frame period.

In 16-line AC drive, WF inverts every 16 lines.

Although 16-line AC drive gives a more readable display, horizontal lines may appear when using high LCD drive voltages or at high viewing angles.

10-1-1-9. FY

Sets the vertical character size as shown in the following table. The height in pixels is equal to FY + 1, where FY can range from 00 to 0FH inclusive.

Set FY to zero (vertical size equals one) when in graphics mode.

HEX	FY				[FY] character height(pixels)
	D3	D2	D1	D0	
00	0	0	0	0	1
01	0	0	0	1	2
	↓	↓	↓	↓	↓
07	0	1	1	1	8
	↓	↓	↓	↓	↓
0E	1	1	1	0	15
0F	1	1	1	1	16

FY

10-1-1-10. C/R

Sets the address range covered by one display line as shown in the following table. The address range is the number of characters less one, multiplied by the number of horizontal bytes per character, and C/R can range from 0 to 239.

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C/R									[C/R] bytes /display line
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
4F	0	1	0	0	1	1	1	1	80
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
EE	1	1	1	0	1	1	1	0	239
EF	1	1	1	0	1	1	1	1	240

10-1-1-11. TC/R

Sets the length, including horizontal blanking of one line as shown in the following table. The line is equal to $TC/R + 1$, where TC/R can range from 0 to 255. TC/R must be greater than or equal to $C/R + 4$.

TC/R									[TC/R] line length (bytes)
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
52	0	1	0	1	0	0	1	0	83
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

10-1-1-12. L/F

Sets the height, in lines, of a frame as shown in the following table. The height in lines is equal to $L/F + 1$, where L/F can range from 0 to 255.

L/F									[L/F] lines / frame
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
7F	0	1	1	1	1	1	1	1	128
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

If W/S is set to 1, thus selecting two-screen display, the number of lines must be even and L/F must, therefore, be an odd number.

10-1-1-13. AP

Defines the horizontal address range of the virtual screen as shown in the following table. APL is the least significant byte of the address.

50h
00h

APL

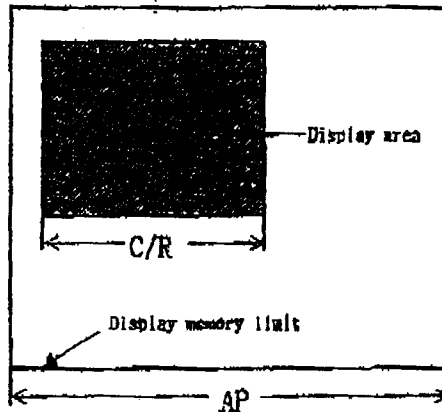
AP7	AP6	AP5	AP4	AP3	AP2	AP1	AP0
-----	-----	-----	-----	-----	-----	-----	-----

APH

AP15	AP14	AP13	AP12	AP11	AP10	AP9	AP8
------	------	------	------	------	------	-----	-----

- AP parameters -

Hex code				[AP] address / line
APH		APL		
0	0	0	0	0
0	0	0	1	1
↓	↓	↓	↓	↓
0	0	5	0	80
↓	↓	↓	↓	↓
F	F	F	E	$2^{16} - 2$
F	F	F	F	$2^{16} - 1$



AP and C/R relationship

10-1-2. SLEEP IN

Puts the device into the sleep state. This command has no parameter bytes.

At least one blank frame after receiving this command, the LCD module halts all internal operations, including the oscillator, and enters the sleep state.

Blank data is sent to the X-drivers, and the Y-drivers have their bias supplies turned off by the YDIS signal. Using the YDIS signal to disable the Y-drivers guards against any spurious displays.

The internal registers of the LCD module maintain their values during the sleep state. The display memory control pins maintain their logic levels to ensure that the display memory is not corrupted.

The LCD module can be removed from the sleep state by sending the SYSTEM SET command with only the P1 parameter. The DISP ON command should be sent next to enable the display.

	MSB						LSB
C	0	1	0	1	0	0	1

-- SLEEP IN command --

1. The YDIS signal goes LOW between one and two frames after the SLEEP IN command is received. Since YDIS forces all display driver outputs to go to the deselected output voltage, YDIS can be used as a power-down signal for the LCD unit. This can be done by having YDIS turn off the relatively high-power LCD drive supplies at the same time as it blanks the display.
2. Since all internal clocks in the LCD module are halted while in the sleep state, a DC voltage will be applied to the LCD panel if the LCD drive supplies remain on. If reliability is a prime consideration, turn off the LCD drive supplies before issuing the SLEEP IN command.
3. Note that, although the bus lines become high impedance in the sleep state, pull-up or pull-down resistors on the bus will force these lines to a known state.

10-2. DISPLAY CONTROL COMMANDS

10-2-1. DISP ON/OFF

Turns the whole display on or off. The single-byte parameter enables and disables the cursor and layered screens, and sets the cursor and screen flash rates. The cursor can be set to flash over one character or over a whole line.

C	<div style="display: flex; justify-content: space-between; font-size: small;"> MSB LSB </div> <div style="display: flex; justify-content: space-around; align-items: center;"> 0 1 0 1 1 0 0 D </div>
P1	FP5 FP4 FP3 FP2 FP1 FP0 FC1 FC0

-- DISP ON/OFF command --

10-2-1-1. D

Turns the display ON or OFF. The D bit takes precedence over the FP bits in the parameter.

D = 0 : Display OFF

D = 1 : Display ON

10-2-1-2. FC

Enables/disables the cursor and sets the flash rate as shown in the following table. The cursor flashes with a 70% duty cycle (ON/OFF).

FC1	FC0		Cursor display
0	0		OFF (blank)
0	1		No flashing
1	0	ON	Flash at $f_{FR}/32\text{Hz}$ (approx. 2 Hz)
1	1		Flash at $f_{FR}/64\text{Hz}$ (approx. 1 Hz)

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10-2-1-3. FP

Each pair of bits in FP sets the attributes of one screen block as shown in the following table.

FP1	FP0	First screen block(SAD1)	
FP3	FP2	Second screen block (SAD2, SAD4). See note.	
FP5	FP4	Third screen block(SAD3)	
0	0	OFF (blank)	
0	1	ON	No flashing
1	0		Flash at $f_{FR}/32\text{Hz}$ (approx. 2 Hz)
1	1		Flash at $f_{FR}/4\text{Hz}$ (approx. 17 Hz)

Note

If SAD4 is enabled by setting W/S to 1, FP3 and FP2 control both SAD2 and SAD4. The attributes of SAD2 and SAD4 cannot be set independently.

10-2-2. SCROLL

10-2-2-1. C

Sets the scroll start address and the number of lines per scroll block as shown in the following table. Parameters P1 to P10 can be omitted if not required.

		MSB							LSB
C		0	1	0	0	0	1	0	0
P1	(SAD 1 L)	A7	A6	A5	A4	A3	A2	A1	A0
P2	(SAD 1 H)	A15	A14	A13	A12	A11	A10	A9	A8
P3	(SL 1)	L7	L6	L5	L4	L3	L2	L1	L0
P4	(SAD 2 L)	A7	A6	A5	A4	A3	A2	A1	A0
P5	(SAD 2 H)	A15	A14	A13	A12	A11	A10	A9	A8
P6	(SL 2)	L7	L6	L5	L4	L3	L2	L1	L0
P7	(SAD 3 L)	A7	A6	A5	A4	A3	A2	A1	A0
P8	(SAD 3 H)	A15	A14	A13	A12	A11	A10	A9	A8
P9	(SAD 4 L)	A7	A6	A5	A4	A3	A2	A1	A0
P10	(SAD 4 H)	A15	A14	A13	A12	A11	A10	A9	A8

(SCROLL COMMAND)

Note

Set the parameter P9 and P10 only if both two-screen drive(W/S=1) and two-layer configuration are selected. SAD4 is the fourth screen block display start address.

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10-2-2-2. SL1, SL2

SL1 and SL2 set the number of lines per scrolling screen, the number of lines is SL1 or SL2, plus one.

SL1, SL2									[S/L] screen lines
HEX	L7	L6	L5	L4	L3	L2	L1	L0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
7F	0	1	1	1	1	1	1	1	128
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

10-2-2-3. CSRFORM

Sets the cursor size and shape. Although the cursor is normally used only in text displays, it can also be used in graphics display when displaying special characters.

	MSB							LSB
C	0	1	0	1	1	1	0	1
P1	0	0	0	0	X3	X2	X1	X0
P2	CM	0	0	0	Y3	Y2	Y1	Y0

(CSRFORM command)

10-2-2-4. CRX

Sets the horizontal size of the cursor from the character origin as shown in the following table. CRX is equal to the cursor size less one. CRX must be less than or equal to FX.

CRX					[CRX] Cursor width (pixels)
HEX	X3	X2	X1	X0	
0	0	0	0	0	1
1	0	0	0	1	2
↓	↓	↓	↓	↓	↓
4	0	1	0	0	9
↓	↓	↓	↓	↓	↓
E	1	1	1	0	15
F	1	1	1	1	16

HYUNDAI

10-2-2-5. CRY

Sets the location of an underscored cursor, in lines, from the character origin as shown in the following table. When using a block cursor, CRY sets the vertical size of the cursor from the character origin. CRY is equal to the number of lines less one.

HEX	CRY				[CRY] Cursor height (lines)
	Y3	Y2	Y1	Y0	
0	0	0	0	0	Illegal
1	0	0	0	1	2
↓	↓	↓	↓	↓	↓
8	1	0	0	0	9
↓	↓	↓	↓	↓	↓
E	1	1	1	0	15
F	1	1	1	1	16

10-2-2-6. CM

Sets the cursor shape. Always set CM to 1 when in graphics mode.

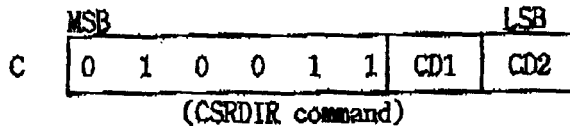
CM = 0 : Underscore cursor

CM = 1 : Block cursor

10-2-3. CSRDIR

Sets the direction of automatic cursor increment as shown in the following table. The cursor can move left or right one character, or up or down by the number or bytes specified by the address pitch, AP.

When reading from and writing to display memory, this automatic cursor increment controls the display memory address increment on each read or write.



C	CD1	CD1	Shift direction
4CH	0	0	Right
4DH	0	1	Left
4EH	1	0	Up
4FH	1	1	Down

10-2-4. OVLAY

Selects layered screen composition and screen text/graphics mode.

	MSB								LSB
C	0	1	0	1	1	0	1	1	
P1	0	0	0	OV	DM2	DM1	MX1	MX0	

(OVLAY command)

10-2-5. CGRAM ADR

Specifies the CG RAM start address.

	MSB								LSB
C	0	1	0	1	1	1	0	0	
P1	A7	A6	A5	A4	A3	A2	A1	A0	(SAGL)
P2	A15	A14	A13	A12	A11	A10	A9	A8	(SAGH)

(CGRAM ADR command)

10-2-6. HDOT SCR

While the SCROLL command only allows scrolling by characters, HDOT SCR allows the screen to be scrolled horizontally by pixels. HDOT SCR cannot be used on individual layers.

	MSB								LSB
C	0	1	0	1	1	0	1	0	
P1	0	0	0	0	0	D2	D1	D0	

(HDOT SCR command)

HEX	P1			Number of pixels to scroll
	D2	D1	D0	
00	0	0	0	0
01	0	0	1	1
02	0	1	0	2
↓	↓	↓	↓	↓
06	1	1	0	6
07	1	1	1	7

10-2-6-1. D0 to D2

Specifies the number of pixels to scroll as shown in the following table. The C/R parameter has to be set to the number of horizontal characters plus one before using HDOT SCR. Smooth scrolling can be simulated if the controlling microprocessor repeatedly issues the HDOT SCR command to the LCD module.

10-3. DRAWING CONTROL COMMANDS

10-3-1. CSRW

The 16bit cursor address register contains the display memory address of the data at the cursor position.

Note that the microprocessor cannot directly access the display memory. The MREAD and MWRITE commands use the address in the register.

	MSB		LSB		
C	0 1 0 0 0 1 1 0				
P1	A7 A6 A5 A4 A3 A2 A1 A0				(CSRL)
P2	A15 A14 A13 A12 A11 A10 A9 A8				(CSRH)
	(CSRW command)				

The cursor address register can only be modified by the CSRW command and by the automatic increment after an MREAD or MWRITE command. It is not affected by display scrolling. If a new address is not set, display memory accesses will be from the last set address or the address after previous automatic increments.

10-3-2. CSRR

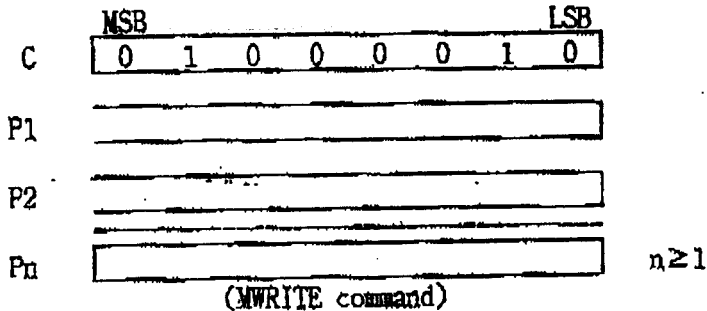
Reads from the cursor address register. After issuing the command, the data read address is read twice, for the low byte and then the high byte of the register.

	MSB		LSB		
C	0 1 0 0 0 1 1 1				
P1	A7 A6 A5 A4 A3 A2 A1 A0				(CSRL)
P2	A15 A14 A13 A12 A11 A10 A9 A8				(CSRH)
	(CSRR command)				

10-4. MEMORY CONTROL COMMANDS

10-4-1. MWRITE

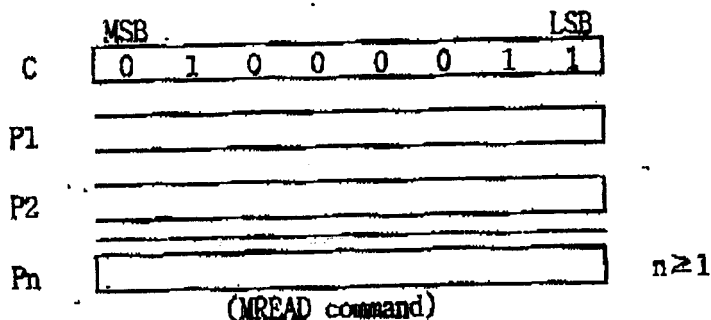
The microprocessor may write a sequence of data bytes to display memory by issuing the MREAD command and then writing the bytes to the LCD module. There is no need for further MWRITE commands for the microprocessor to update the cursor address register after each byte as the cursor address is automatically incremented by the amount set with CSRDIR, in preparation for the next data write.



Note
P1, P2, ..., Pn : Display data

10-4-2. MREAD

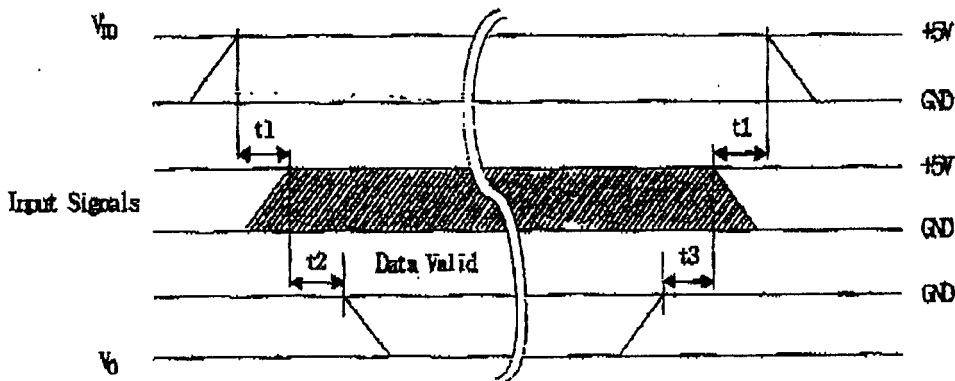
Puts the LCD module into the data output state. On the MREAD command, the display memory data at the cursor address is read into a buffer in the LCD module. Each time the microprocessor reads the buffer the cursor address is incremented by the amount set by CSRDIR and the next data byte fetched from memory, so a sequence of data bytes can be read without further MREAD commands or by updating the cursor address register. If the cursor is displayed, the read data will be from two positions ahead of the cursor.



11. POWER ON/OFF AND SIGNAL INPUT TIMING

Power ON/OFF and signal input should be performed according to the timing shown in the figure below in order not to damage the LCD driving circuit and the LCD panel.

ITEM	Min.	Max.	Unit
t1	0	20	ms
t2	20	-	ms
t3	0	-	ms



12. RELATION BETWEEN DATA AND DISPLAY

